60V Current Mode Synchronous Step-Up Controller

FEATURES

- **High Output Voltages: Up to 60V**
- **Large 1Ω Gate Drivers**
- **No Current Sense Resistor Required**
- **Dual N-Channel MOSFET Synchronous Drive**
- ±0.5% 0.8V Voltage Reference
- Fast Transient Response
- Programmable Soft-Start
- Generates 5.5V Driver Supply
- Power Good Output Voltage Monitor
- Adjustable Off-Time/Frequency: $t_{OFF(MIN)}$ < 100ns
- Adjustable Cycle-by-Cycle Current Limit
- Undervoltage Lockout On Driver Supply
- Output Overvoltage Protection
- Thermally Enhanced 16-Pin TSSOP Package

APPLICATIONS

- 24V Fan Supplies
- 48V Telecom and Base Station Power Supplies
- Networking Equipment, Servers
- Automotive and Industrial Control Systems

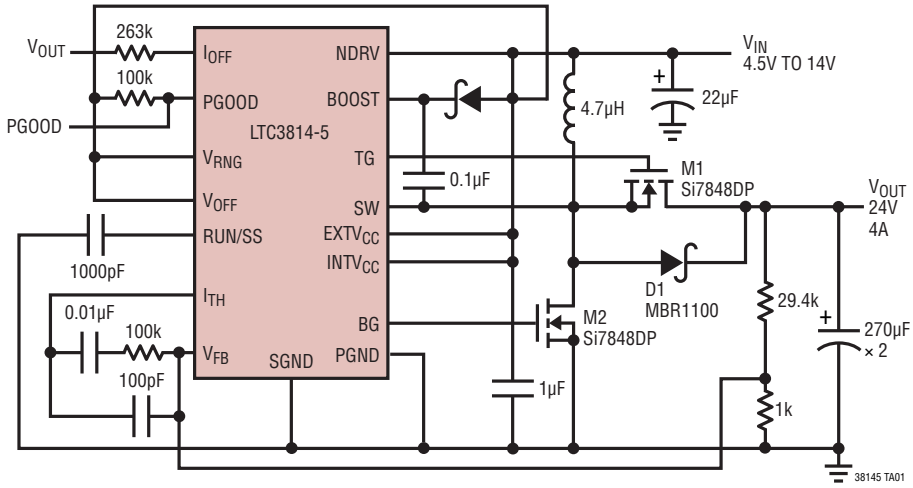
DESCRIPTION

The LTC3814-5 is a synchronous step-up switching regulator controller that can generate output voltages up to 60V. The LTC3814-5 uses a constant off-time peak current control architecture to deliver very high duty cycles with accurate cycle-by-cycle current limit without requiring a sense resistor.

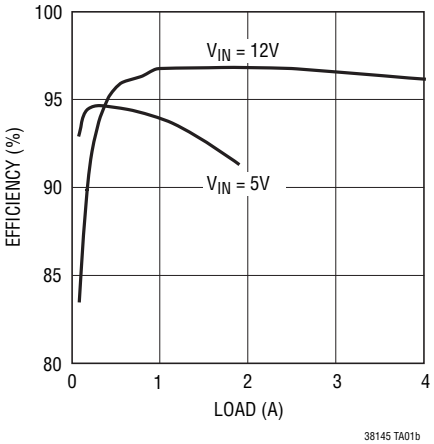
A precise internal reference provides ±0.5% DC accuracy. A high bandwidth (25MHz) error amplifier provides very fast line and load transient response. Large 1Ω gate drivers allow the LTC3814-5 to drive large power MOSFETs for higher current applications. The operating frequency is selected by an external resistor and is compensated for variations in V_{IN}. A shutdown pin allows the LTC3814-5 to be turned off reducing the supply current to <230µA.

TYPICAL APPLICATION

High Efficiency High Voltage Step-Up Converter



Efficiency vs Load Current



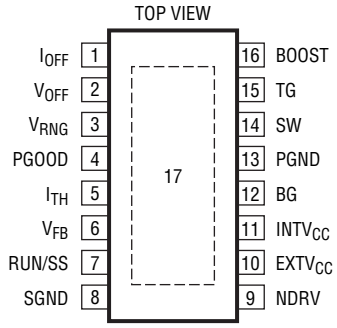
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
- $INTV_{CC}$ ..... –0.3V to 14V
- ($INTV_{CC}$ – PGND), (BOOST – SW) ..... –0.3V to 14V
- BOOST (Continuous) ..... –0.3V to 85V
- BOOST (≤400ms) ..... –0.3V to 95V
- $EXTV_{CC}$ ..... –0.3V to 15V
- ($EXTV_{CC}$ – $INTV_{CC}$)..... –12V to 12V

($NDRV – INTV_{CC}$) Voltage..... –0.3V to 10V
SW Voltage (Continuous)..... –1V to 70V
SW Voltage (400ms)..... –1V to 80V
I_{OFF} Voltage (Continuous) ..... –0.3V to 70V
I_{OFF} Voltage (400ms) ..... –0.3V to 80V
RUN/SS Voltage..... –0.3V to 5V
PGOOD Voltage..... –0.3V to 7V
V_{RNG}, V_{OFF} Voltages..... –0.3V to 14V
FB Voltage..... –0.3V to 2.7V
TG, BG, $INTV_{CC}$, $EXTV_{CC}$ RMS Currents.....50mA
Operating Junction Temperature Range
(Notes 2, 3, 7)..... –40°C to 125°C
Storage Temperature Range.....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3814EFE-5#PBF	LTC3814EFE-5#TRPBF	3814EFE-5	16-Lead Plastic TSSOP	–40°C to 125°C
LTC3814IFE-5#PBF	LTC3814IFE-5#TRPBF	3814IFE-5	16-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), $INTV_{CC}$ = V_{BOOST} = V_{RNG} = V_{EXTVCC} = V_{NDRV} = V_{OFF} = 5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
$INTV_{CC}$	$INTV_{CC}$ Supply Voltage		●	4.35		14	V
I_Q	$INTV_{CC}$ Supply Current $INTV_{CC}$ Shutdown Current	RUN/SS > 1.5V (Notes 4, 5) RUN/SS = 0V			3 224	6 600	mA µA
I_{BOOST}	BOOST Supply Current	RUN/SS > 1.5V (Note 5) RUN/SS = 0V			240 0	400 5	µA µA
V_{FB}	Feedback Voltage	(Note 4) 0°C to 85°C –40°C to 85°C –40°C to 125°C	 ● ● ●	0.796 0.794 0.792 0.792	0.800 0.800 0.800 0.800	0.804 0.806 0.806 0.808	V V V V
$\Delta V_{FB,LINE}$	Feedback Voltage Line Regulation	5V < $INTV_{CC}$ < 14V (Note 4)	●		0.002	0.02	%/V
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{RNG} = 2V, V_{FB} = 0.76V V_{RNG} = 0V, V_{FB} = 0.76V V_{RNG} = $INTV_{CC}$, V_{FB} = 0.76V		256 70 170	320 95 215	384 120 260	mV mV mV
$V_{SENSE(MIN)}$	Minimum Current Sense Threshold	V_{RNG} = 2V, V_{FB} = 0.84V V_{RNG} = 0V, V_{FB} = 0.84V V_{RNG} = $INTV_{CC}$, V_{FB} = 0.84V			–300 –85 –200		mV mV mV
I_{VFB}	Feedback Current	V_{FB} = 0.8V			20	150	nA
A_{VOL}(EA)	Error Amplifier DC Open-Loop Gain			65	100		dB
f_U	Error Amp Unity Gain Crossover Frequency	(Note 6)			25		MHz
$V_{RUN/SS}$	Shutdown Threshold			0.6	0.9	1.2	V
$I_{RUN/SS}$	RUN/SS Source Current	RUN/SS = 0V		0.7	1.4	2.5	µA
V_{VCCUV}	$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Rising Hysteresis	●	4.05	4.2 0.5	4.35	V V
Oscillator							
t_{OFF}	Off-Time	I_{OFF} = 100µA I_{OFF} = 300µA		1.55 515	1.85 605	2.15 695	µs ns
$t_{OFF(MIN)}$	Minimum Off-Time	I_{OFF} = 2000µA				100	ns
$t_{ON(MIN)}$	Minimum On-Time				350		ns
Driver							
$I_{BG,PEAK}$	BG Driver Peak Source Current	V_{BG} = 0V		0.7	1		A
$R_{BG,SINK}$	BG Driver Pulldown $R_{DS(ON)}$				1	1.5	Ω
$I_{TG,PEAK}$	TG Driver Peak Source Current	V_{TG} – V_{SW} = 0V		0.7	1		A
$R_{TG,SINK}$	TG Driver Pulldown $R_{DS(ON)}$				1	1.5	Ω
PGOOD Output							
ΔV_{FBOV}	PGOOD Upper Threshold PGOOD Lower Threshold	V_{FB} Rising V_{FB} Falling		7.5 –7.5	10 –10	12.5 –12.5	% %
$\Delta V_{FB,HYST}$	PGOOD Hysteresis	V_{FB} Returning			1.5	3	%
V_{PGOOD}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.3	0.6	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V			0	2	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), $INTV_{CC}$ = V_{BOOST} = V_{RNG} = V_{EXTVCC} = V_{NDRV} = V_{OFF} = 5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PG Delay	PGOOD Delay	V_{FB} Falling			125		µs
V_{CC} Regulators							
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage $EXTV_{CC}$ Rising $EXTV_{CC}$ Hysteresis		● ●	4.5 0.1	4.7 0.25	 0.4	V V
$V_{INTVCC,1}$	$INTV_{CC}$ Voltage from $EXTV_{CC}$	6V < V_{EXTVCC} < 15V		5.2	5.5	5.8	V
$\Delta V_{EXTVCC,1}$	V_{EXTVCC} - V_{INTVCC} at Dropout	I_{CC} = 20mA, V_{EXTVCC} = 5V			75	150	mV
$\Delta V_{LOADREG,1}$	$INTV_{CC}$ Load Regulation from $EXTV_{CC}$	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 10V			0.01		%
$V_{INTVCC,2}$	$INTV_{CC}$ Voltage from NDRV Regulator	Linear Regulator in Operation		5.2	5.5	5.8	V
$\Delta V_{LOADREG,2}$	$INTV_{CC}$ Load Regulation from NDRV	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 0			0.01		%
I_{NDRV}	Current into NDRV Pin	V_{NDRV} – V_{INTVCC} = 3V		20	40	60	µA
V_{CCSR}	Maximum Supply Voltage	Trickle Charger Shunt Regulator			15		V
I_{CCSR}	Maximum Current into NDRV/$INTV_{CC}$	Trickle Charger Shunt Regulator, $INTV_{CC}$ ≤ 16.7V (Note 8)		10			mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3814-5 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3814E-5 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3814I-5 is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC3814-5: $T_J = T_A + (P_D \bullet 38°C/W)$

Note 4: The LTC3814-5 is tested in a feedback loop that servos V_{FB} to the reference voltage with the I_{TH} pin forced to a voltage between 1V and 2V.

Note 5: The dynamic input supply current is higher due to the power MOSFET gate charging being delivered at the switching frequency ($Q_G \bullet f_{SW}$).

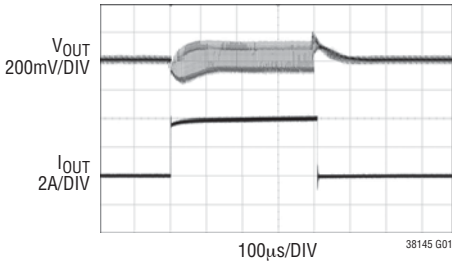
Note 6: Guaranteed by design. Not subject to test.

Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 8: I_{CC} is the sum of current into NDRV and $INTV_{CC}$.

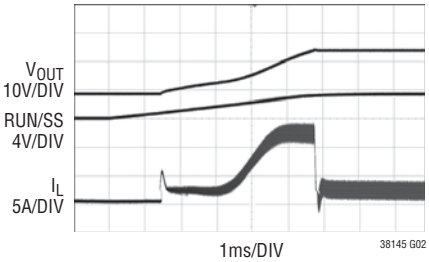
TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient Response



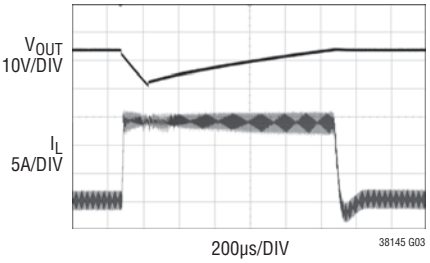
FRONT PAGE CIRCUIT
V_{IN} = 12V
0A TO 4A LOAD STEP

Start-Up



FRONT PAGE CIRCUIT
V_{IN} = 12V
I_{LOAD} = 1A

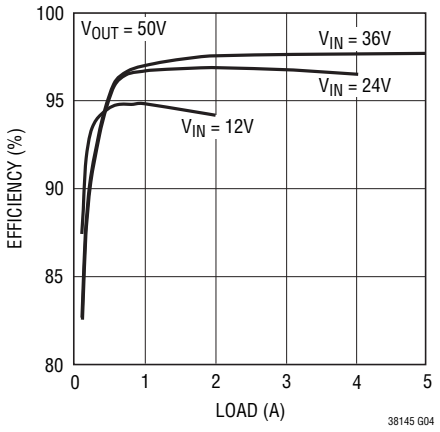
Overcurrent Operation



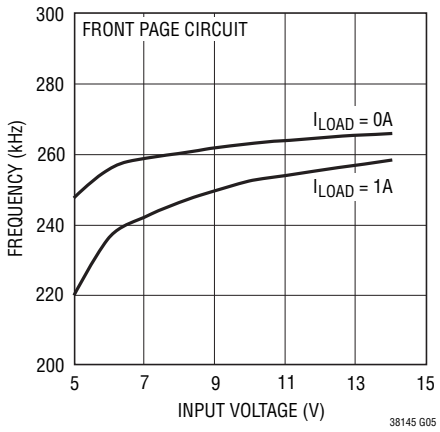
FRONT PAGE CIRCUIT
V_{IN} = 12V
V_{RNG} = 1V
R_{SHORT} = 1Ω

TYPICAL PERFORMANCE CHARACTERISTICS

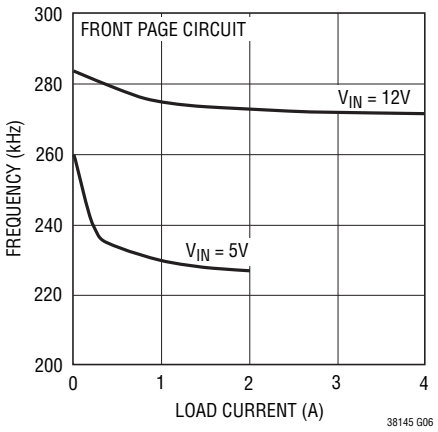
Efficiency vs Load Current



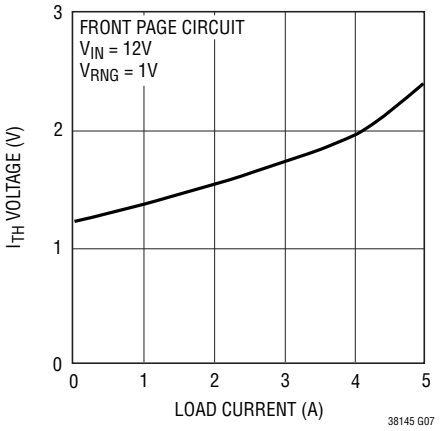
Frequency vs Input Voltage



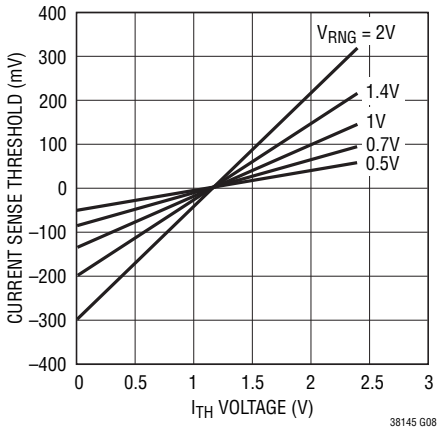
Frequency vs Load Current



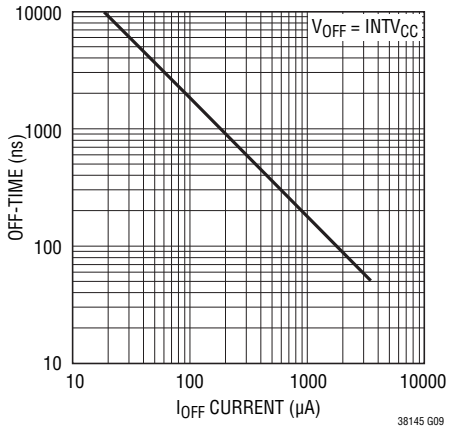
ITH Voltage vs Load Current



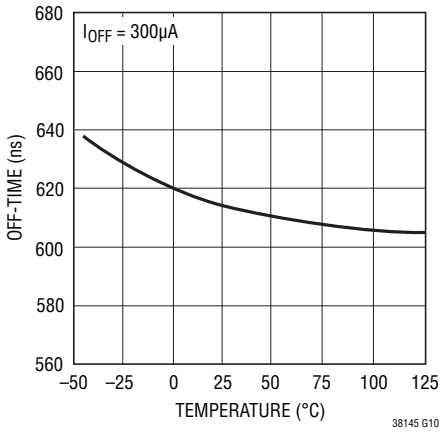
Current Sense Threshold vs ITH Voltage



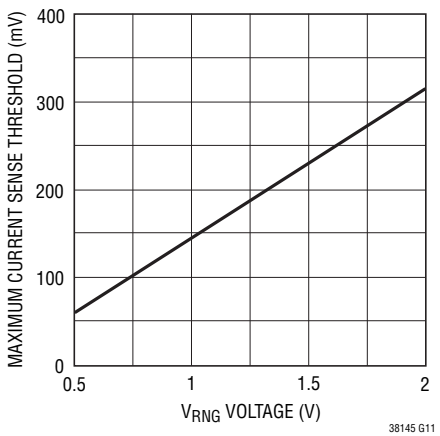
Off-Time vs IOFF Current



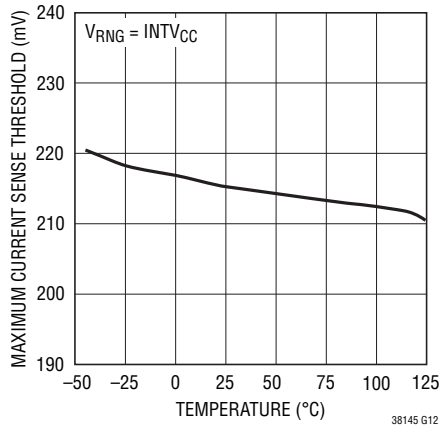
Off-Time vs Temperature



Maximum Current Sense Threshold vs VRNG Voltage

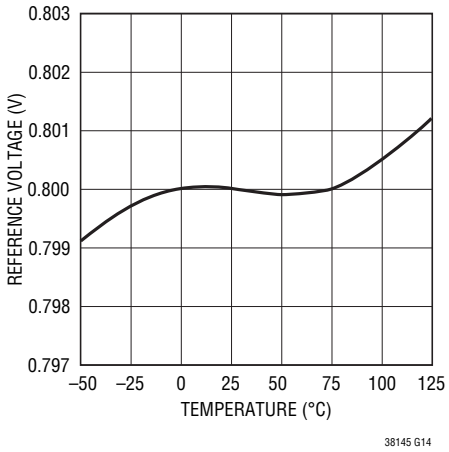


Maximum Current Sense Threshold vs Temperature

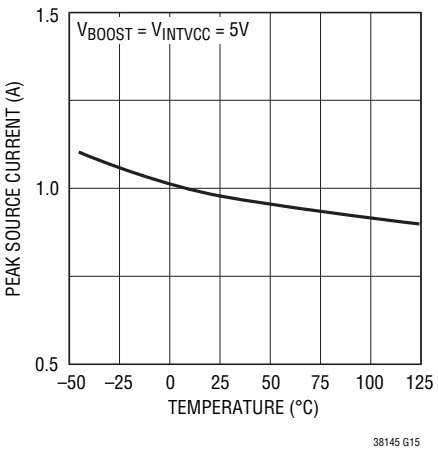


TYPICAL PERFORMANCE CHARACTERISTICS

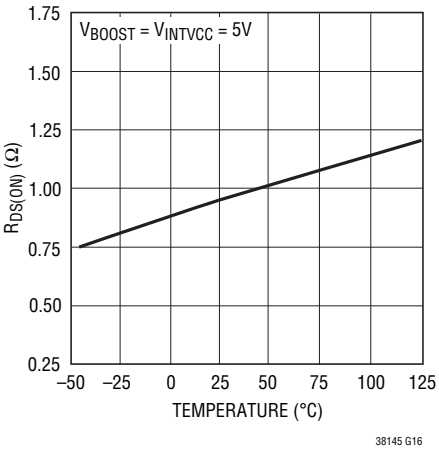
Reference Voltage vs Temperature



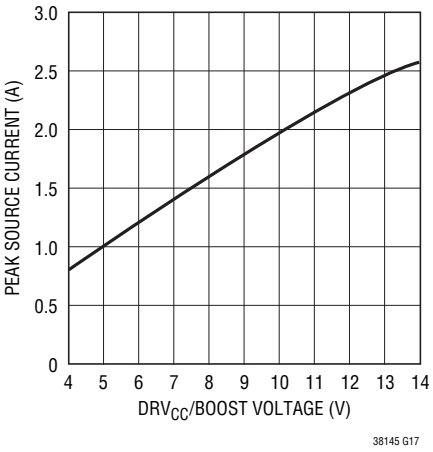
Driver Peak Source Current vs Temperature



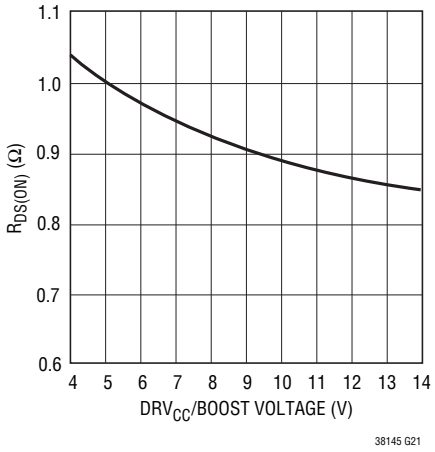
Driver Pulldown $R_{DS(ON)}$ vs Temperature



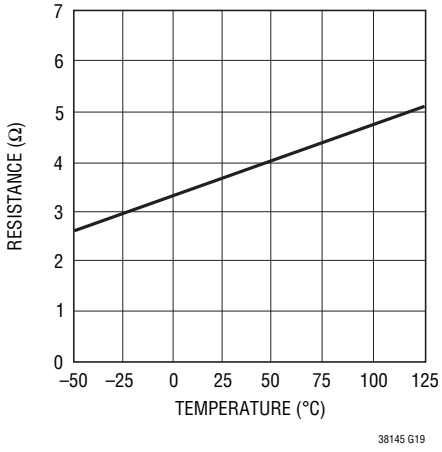
Driver Peak Source Current vs Supply Voltage



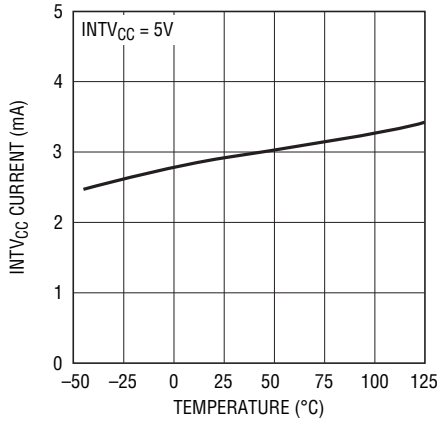
Driver Pulldown $R_{DS(ON)}$ vs Supply Voltage



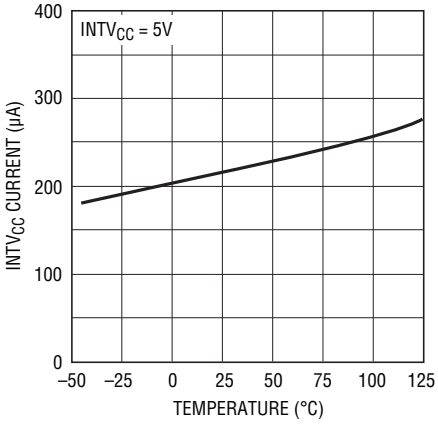
$EXTV_{CC}$ Switch Resistance vs Temperature



$INTV_{CC}$ Current vs Temperature

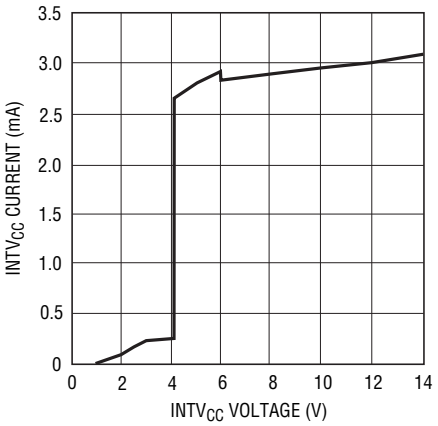


$INTV_{CC}$ Shutdown Current vs Temperature

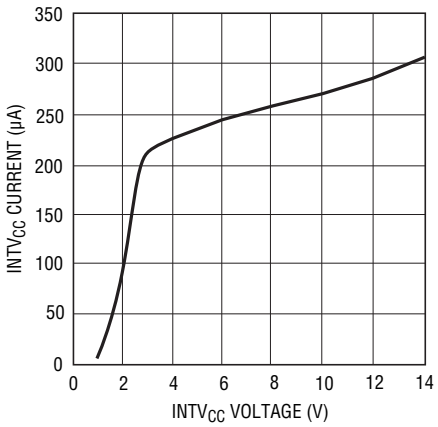


TYPICAL PERFORMANCE CHARACTERISTICS

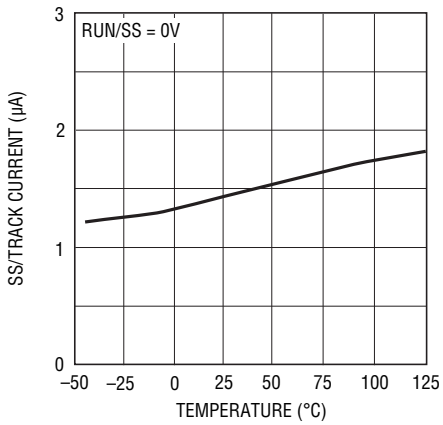
$INTV_{CC}$ Current vs $INTV_{CC}$ Voltage



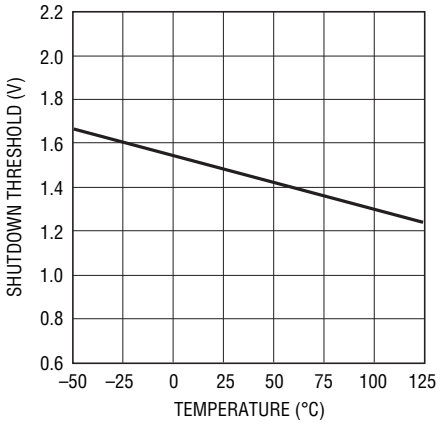
$INTV_{CC}$ Shutdown Current vs $INTV_{CC}$ Voltage



RUN/SS Pull-Up Current vs Temperature



Shutdown Threshold vs Temperature



PIN FUNCTIONS

I_{OFF} (Pin 1): Off-Time Current Input. Tie a resistor from V_{OUT} to this pin to set the one-shot timer current and thereby set the switching frequency.

V_{OFF} (Pin 2): Off-Time Voltage Input. Voltage trip point for the on-time comparator. Tying this pin to an external resistive divider from the input makes the off-time proportional to V_{IN}. The comparator defaults to 0.7V when the pin is grounded and defaults to 2.4V when the pin is connected to $INTV_{CC}$.

V_{RNG} (Pin 3): Sense Voltage Limit Set. The voltage at this pin sets the nominal sense voltage at maximum output current and can be set from 0.5V to 2V by a resistive divider from $INTV_{CC}$. The nominal sense voltage defaults to 95mV when this pin is tied to ground, and 215mV when tied to $INTV_{CC}$.

PGOOD (Pin 4): Power Good Output. Open-drain logic output that is pulled to ground when the output voltage is not between ±10% of the regulation point. The output voltage must be out of regulation for at least 125µs before the power good output is pulled to ground.

I_{TH} (Pin 5): Error Amplifier Compensation Point and Current Control Threshold. The current comparator threshold increases with control voltage. The voltage ranges from 0V to 2.6V with 1.2V corresponding to zero sense voltage (zero current).

V_{FB} (Pin 6): Feedback Input. Connect V_{FB} through a resistor divider network to V_{OUT} to set the output voltage.

RUN/SS (Pin 7): RUN/Soft-Start Input. For soft-start, a capacitor to ground at this pin sets the ramp rate of the maximum current sense threshold. Pulling this pin below 0.9V will shut down the LTC3814-5, turn off both of the external MOSFET switches and reduce the quiescent supply current to 224µA.

SGND (Pin 8): Signal Ground. All small-signal components should connect to this ground and eventually connect to PGND at one point.

NDRV (Pin 9): Drive Output for External Pass Device of the Linear Regulator for $INTV_{CC}$. Connect to the gate of an external NMOS pass device and a pull-up resistor to the input voltage V_{IN} or the output voltage V_{OUT}.

$EXTV_{CC}$ (Pin 10): External Driver Supply Voltage. When this voltage exceeds 4.7V, an internal switch connects this pin to $INTV_{CC}$ through an LDO and turns off the external MOSFET connected to NDRV, so that controller and gate drive are drawn from $EXTV_{CC}$.

$INTV_{CC}$ (Pin 11): Main Supply and Driver Supply Pin. All internal circuits and bottom gate output driver are powered from this pin. $INTV_{CC}$ should be bypassed to SGND and PGND with a low ESR (X5R or better) 1µF capacitor in close proximity to the LTC3814-5.

BG (Pin 12): Bottom Gate Drive. The BG pin drives the gate of the bottom N-channel main switch MOSFET. This pin swings from PGND to $INTV_{CC}$.

PGND (Pin 13): Bottom Gate Return. This pin connects to the source of the pull-down MOSFET in the BG driver and is normally connected to ground.

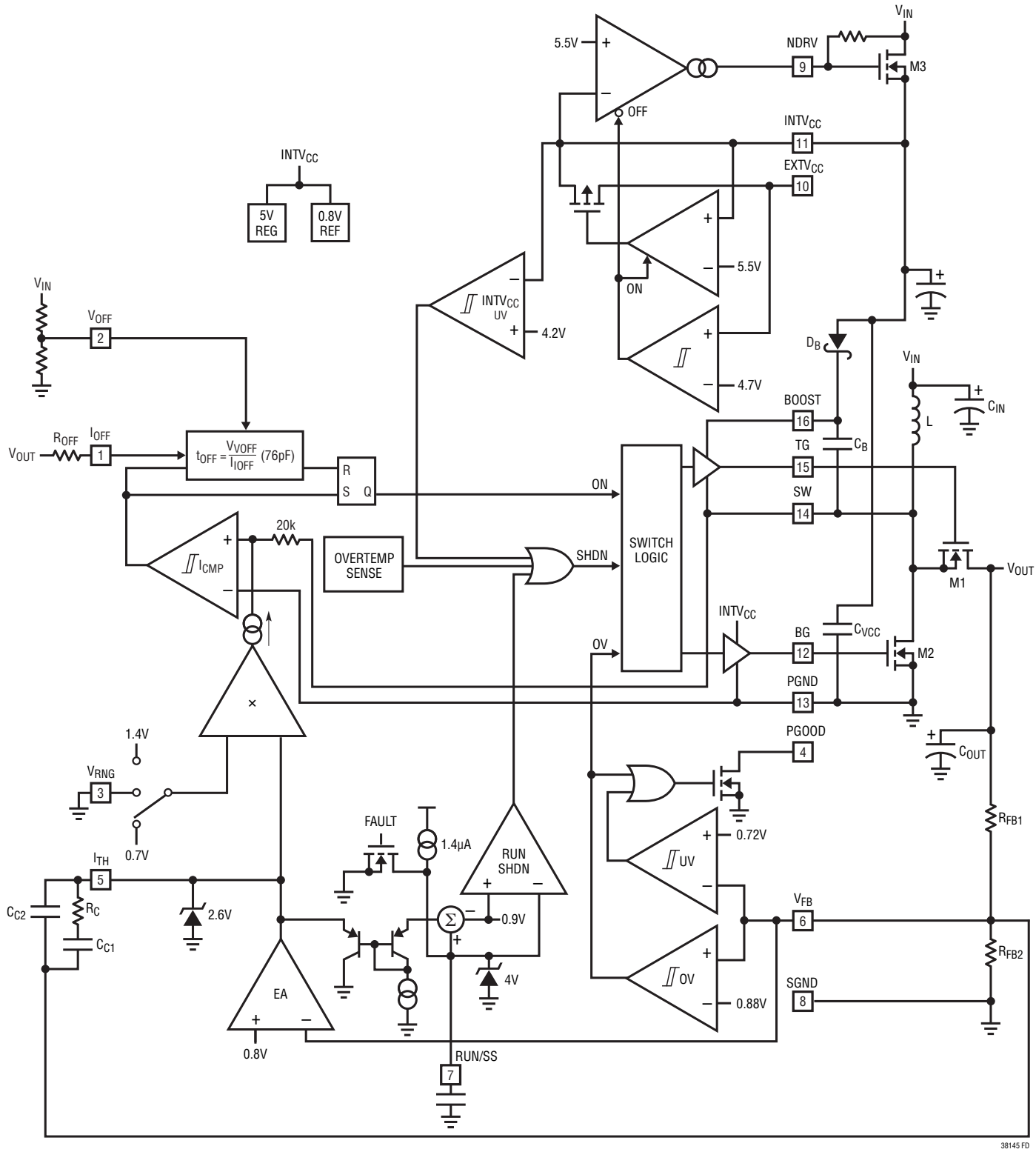
SW (Pin 14): Switch Node Connection to Inductor and Bootstrap Capacitor. Voltage swing at this pin is from a Schottky diode (external) voltage drop below ground to V_{OUT}.

TG (Pin 15): Top Gate Drive. The TG pin drives the gate of the top N-channel synchronous switch MOSFET. The TG driver draws power from the BOOST pin and returns to the SW pin, providing true floating drive to the top MOSFET.

BOOST (Pin 16): Top Gate Driver Supply. The BOOST pin supplies power to the floating TG driver. BOOST should be bypassed to SW with a low ESR (X5R or better) 0.1µF capacitor. An additional fast recovery diode from $INTV_{CC}$ to the BOOST pin will create a complete floating charge-pumped supply at BOOST.

GND (Exposed Pad Pin 17): Ground. The Exposed Pad must be soldered to PCB ground.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3814-5 is a current mode controller for DC/DC step-up converters. In normal operation, the top MOSFET is turned on for a fixed interval determined by a one-shot timer (OST). When the top MOSFET is turned off, the bottom MOSFET is turned on until the current comparator I_{CMP} trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage between the PGND and SW pins using the bottom MOSFET on-resistance. The voltage on the I_{TH} pin sets the comparator threshold corresponding to the inductor peak current. The fast 25MHz error amplifier EA adjusts this voltage by comparing the feedback signal V_{FB} to the internal 0.8V reference voltage. If the load current increases, it causes a drop in the feedback voltage relative to the reference. The I_{TH} voltage then rises until the average inductor current again matches the load current.

The operating frequency is determined implicitly by the top MOSFET on-time (t_{OFF}) and the duty cycle required to maintain regulation. The one-shot timer generates a top MOSFET on-time that is inversely proportional to the I_{OFF} current and proportional to the V_{OFF} voltage. Connecting V_{OUT} to I_{OFF} and V_{IN} to V_{OFF} with a resistive divider keeps the frequency approximately constant with changes in V_{IN}. The nominal frequency can be adjusted with an external resistor R_{OFF}.

Pulling the RUN/SS pin low forces the controller into its shutdown state, turning off both M1 and M2. Forcing a voltage above 0.9V will turn on the device.

Fault Monitoring/Protection

Constant off-time current mode architecture provides accurate cycle-by-cycle current limit protection—a feature that is very important for protecting the high voltage power supply from output overcurrent conditions. The cycle-by-cycle current monitor guarantees that the inductor current will never exceed the value programmed on the V_{RNG} pin.

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point after the internal 125µs power bad mask timer expires. Furthermore, in an overvoltage condition, M2 is turned off and M1 is turned on immediately and held on until the overvoltage condition clears.

The LTC3814-5 provides an undervoltage lockout comparator for the $INTV_{CC}$ supply. The $INTV_{CC}$ UV threshold is 4.2V to guarantee that the MOSFETs have sufficient gate drive voltage before turning on. If $INTV_{CC}$ is under the UV threshold, the LTC3814-5 is shut down and the drivers are turned off.

Strong Gate Drivers

The LTC3814-5 contains very low impedance drivers capable of supplying amps of current to slew large MOSFET gates quickly. This minimizes transition losses and allows paralleling MOSFETs for higher current applications. A 60V floating high side driver drives the topside MOSFET and a low side driver drives the bottom side MOSFET (see Figure 1). The bottom side driver is supplied directly from the $INTV_{CC}$ pin. The top MOSFET drivers are biased from floating bootstrap capacitor C_B, which normally is recharged during each off cycle through an external diode from $INTV_{CC}$ when the top MOSFET turns off. In an output overvoltage condition, where it is possible that the bottom MOSFET will be off for an extended period of time, an internal timeout guarantees that the bottom MOSFET is turned on at least once every 25µs for one top MOSFET on-time period to refresh the bootstrap capacitor.

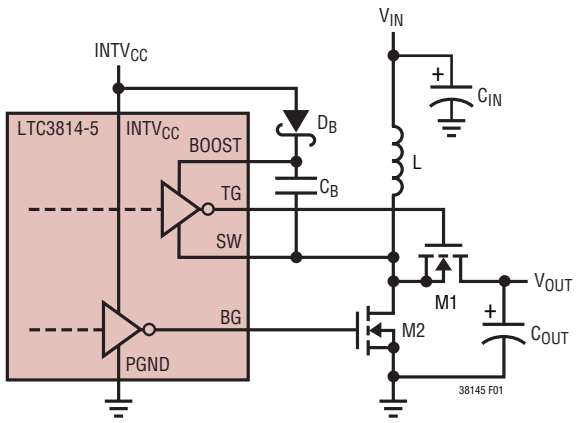


Figure 1. Floating TG Driver Supply and Negative BG Return

OPERATION

IC/Driver Supply Power

The LTC3814-5's internal control circuitry and top and bottom MOSFET drivers operate from a supply voltage ($INTV_{CC}$ pin) in the range of 4.5V to 14V. If the input supply voltage or another available supply is within this voltage range it can be used to supply IC/driver power. If a supply in this range is not available, two internal regulators are available to generate a 5.5V supply from the input or output. An internal low dropout regulator is good for voltages up to 15V, and the second, a linear regulator controller, controls the gate of an external NMOS to generate the 5.5V supply. Since the NMOS is external, the user has the flexibility to choose a BV_{DSS} as high as necessary.

APPLICATIONS INFORMATION

The basic LTC3814-5 application circuit is shown on the first page of this data sheet. External component selection is primarily determined by the maximum input voltage and load current and begins with the selection of the power MOSFET switches. The LTC3814-5 uses the on-resistance of the synchronous power MOSFET for determining the inductor current. The desired amount of ripple current and operating frequency largely determines the inductor value. Next, C_{OUT} is selected for its ability to handle the large RMS current and is chosen with low enough ESR to meet the output voltage ripple and transient specification. Finally, loop compensation components are selected to meet the required transient/phase margin specifications.

Duty Cycle Considerations

For a boost converter, the duty cycle of the main switch is:

$$D = 1 - \frac{V_{IN}}{V_{OUT}}; D_{MAX} = 1 - \frac{V_{IN(MIN)}}{V_{OUT}}$$

The maximum V_{OUT} capability of the LTC3814-5 is inversely proportional to the minimum desired operating frequency and minimum off-time:

$$V_{OUT(MAX)} = \frac{V_{IN(MIN)}}{f_{MIN} \bullet t_{OFF(MIN)}} \leq 60V$$

Maximum Sense Voltage and the V_{RNG} Pin

The control circuit in the LTC3814-5 measures the input current by using the $R_{DS(ON)}$ of the bottom MOSFET or by using a sense resistor in the bottom MOSFET source, so the output current needs to be reflected back to the input in order to dimension the power MOSFET properly and to choose the maximum sense voltage. Based on the fact that, ideally, the output power is equal to the input power, the maximum average input current and average inductor current is:

$$I_{IN(MAX)} = I_{L,AVG(MAX)} = \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The current mode control loop will not allow the inductor peak to exceed $V_{SENSE(MAX)}/R_{SENSE}$. In practice, one should allow some margin for variations in the LTC3814-5 and external component values, and a good guide for selecting the maximum sense voltage when V_{DS} sensing is used is:

$$V_{SENSE(MAX)} = \frac{1.7 \bullet R_{DS(ON)} \bullet I_{O(MAX)}}{1 - D_{MAX}}$$

V_{SENSE} is set by the voltage applied to the V_{RNG} pin. Once V_{SENSE} is chosen, the required V_{RNG} voltage is calculated to be:

$$V_{RNG} = 5.78 \bullet (V_{SENSE(MAX)} + 0.026)$$

An external resistive divider from $INTV_{CC}$ can be used to set the voltage of the V_{RNG} pin between 0.5V and 2V resulting in nominal sense voltages of 60mV to 320mV. Additionally, the V_{RNG} pin can be tied to SGND or $INTV_{CC}$ in which case the nominal sense voltage defaults to 95mV or 215mV, respectively.

APPLICATIONS INFORMATION

Power MOSFET Selection

The LTC3814-5 requires two external N-channel power MOSFETs, one for the bottom (main) switch and one for the top (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage BV_{DSS}, threshold voltage $V_{(GS)TH}$, on-resistance $R_{DS(ON)}$, Miller capacitance and maximum current $I_{DS(MAX)}$.

Since the bottom MOSFET is used as the current sense element, particular attention must be paid to its on-resistance. MOSFET on-resistance is typically specified with a maximum value $R_{DS(ON)(MAX)}$ at 25°C. In this case, additional margin is required to accommodate the rise in MOSFET on-resistance with temperature:

$$R_{DS(ON)(MAX)} = \frac{R_{SENSE}}{\rho_T}$$

The ρ_T term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature (see Figure 2) and typically varies from 0.4%/°C to 1.0%/°C depending on the particular MOSFET used.

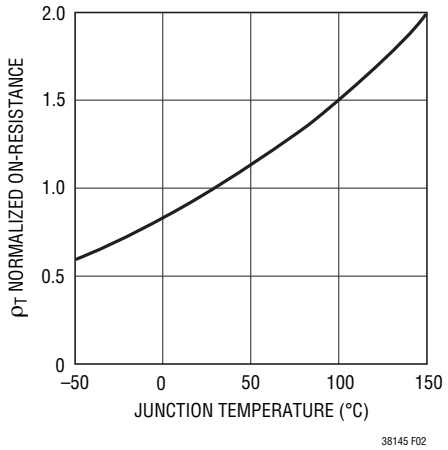


Figure 2. $R_{DS(ON)}$ vs Temperature

The most important parameter in high voltage applications is breakdown voltage BV_{DSS}. Both the top and bottom MOSFETs will see full output voltage plus any additional ringing on the switch node across its drain-to-source during its off-time and must be chosen with the appropriate breakdown specification. The LTC3814-5 is designed to be used with a 4.5V to 14V gate drive supply ($INTV_{CC}$ pin) for driving logic-level MOSFETs ($V_{GS(MIN)} \geq 4.5V$).

For maximum efficiency, on-resistance $R_{DS(ON)}$ and input capacitance should be minimized. Low $R_{DS(ON)}$ minimizes conduction losses and low input capacitance minimizes transition losses. MOSFET input capacitance is a combination of several components but can be taken from the typical "gate charge" curve included on most data sheets (Figure 3).

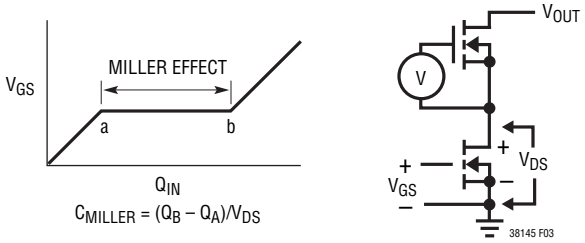


Figure 3. Gate Charge Characteristic

The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying by the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturers data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included.

APPLICATIONS INFORMATION

When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}}$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{MAIN} = D_{MAX}\left(\frac{I_{O(MAX)}}{1-D_{MAX}}\right)^2(\rho_T)R_{DS(ON)} + \frac{1}{2}V_{OUT}{}^2\left(\frac{I_{O(MAX)}}{1-D_{MAX}}\right)(R_{DR})(C_{MILLER}) \bullet \left[\frac{1}{INTV_{CC}-V_{TH(IL)}} + \frac{1}{V_{TH(IL)}}\right](f)$$

$$P_{SYNC} = \left(\frac{1}{1-D_{MAX}}\right)(I_{O(MAX)})^2(\rho_T)\,R_{DS(0N)}$$

where ρ_T is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$). $V_{TH(IL)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

Both MOSFETs have I^2R losses while the bottom N-channel equation includes an additional term for transition losses. Both top and bottom MOSFET I^2R losses are greatest at lowest V_{IN}, and the top MOSFET I^2R losses also peak during an overcurrent condition when it is on close to 100% of the period. For most LTC3814-5 applications, the transition loss and I^2R loss terms in the bottom MOSFET are comparable, so best efficiency is obtained by choosing a MOSFET that optimizes both $R_{DS(ON)}$ and C_{MILLER}. Since there is no transition loss term in the synchronous MOSFET, however, optimal efficiency is obtained by minimizing $R_{DS(ON)}$—by using larger MOSFETs or paralleling multiple MOSFETs.

Multiple MOSFETs can be used in parallel to lower $R_{DS(ON)}$ and meet the current and thermal requirements if desired. The LTC3814-5 contains large low impedance drivers capable of driving large gate capacitances without significantly slowing transition times. In fact, when driving MOSFETs with very low gate charge, it is sometimes helpful to slow down the drivers by adding small gate resistors (10Ω or less) to reduce noise and EMI caused by the fast transitions.

Operating Frequency

The choice of operating frequency is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance in order to maintain low output ripple voltage.

The operating frequency of LTC3814-5 applications is determined implicitly by the one-shot timer that controls the on-time t_{OFF} of the synchronous MOSFET switch. The on-time is set by the current into the I_{OFF} pin and the voltage at the V_{OFF} pin according to:

$$t_{OFF} = \frac{V_{VOFF}}{I_{IOFF}}(76pF)$$

Tying a resistor R_{OFF} from V_{OUT} to the I_{OFF} pin yields a synchronous MOSFET on-time inversely proportional to V_{OUT}. This results in the following operating frequency and also keeps frequency constant as V_{OUT} ramps up at start-up:

$$f = \frac{V_{IN}}{V_{VOFF} \bullet R_{OFF}\,(76pF)}\,(Hz)$$

The V_{OFF} pin can be connected to $INTV_{CC}$ or ground or can be connected to a resistive divider from V_{IN}. The V_{OFF} pin has internal clamps that limit its input to the one-shot timer. If the pin is tied below 0.7V, the input to the one-shot is clamped at 0.7V. Similarly, if the pin is tied above 2.4V, the input is clamped at 2.4V. **Note, however, that if the V_{OFF} pin is connected to a constant voltage, the operating frequency will be proportional to the input voltage V_{IN}.** Figures 4a and 4b illustrate how R_{OFF} relates to switching frequency as a function of the input voltage and V_{OFF} voltage. To hold frequency constant for input

APPLICATIONS INFORMATION

voltage changes, tie the V_{OFF} pin to a resistive divider from V_{IN}, as shown in Figure 5. Choose the resistor values so that the V_{RNG} voltage equals about 1.55V at the mid-point of V_{IN} as follows:

$$V_{IN,MID} = \frac{V_{IN(MAX)} + V_{IN(MIN)}}{2} = 1.55V \bullet \left(1 + \frac{R1}{R2}\right)$$

With these resistor values, the frequency will remain relatively constant at:

$$f = \frac{1 + R1/R2}{R_{OFF}(76pF)} (Hz)$$

for the range of $0.45V_{IN}$ to $1.55 \bullet V_{IN}$, and will be proportional to V_{IN} outside of this range.

Changes in the load current magnitude will also cause a frequency shift. Parasitic resistance in the MOSFET switches and inductor reduce the effective voltage across the inductance, resulting in increased duty cycle as the load current increases. By shortening the off-time slightly as current increases, constant-frequency operation can be maintained. This is accomplished with a resistor connected from the I_{TH} pin to the I_{OFF} pin to increase the I_{OFF} current slightly as V_{ITH} increases. The values required will depend on the parasitic resistances in the specific application. A good starting point is to feed about 10% of the R_{OFF} current with R_{ITH} as shown in Figure 6.

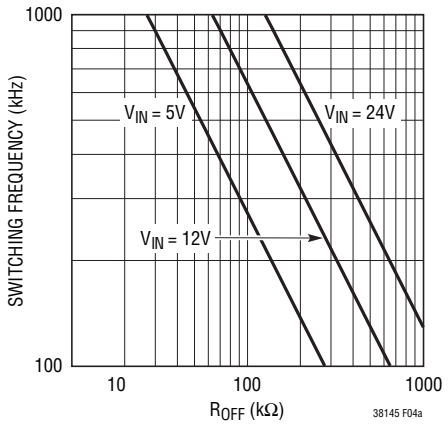


Figure 4a. Switching Frequency vs R_{OFF} (V_{OFF} = $INTV_{CC}$)

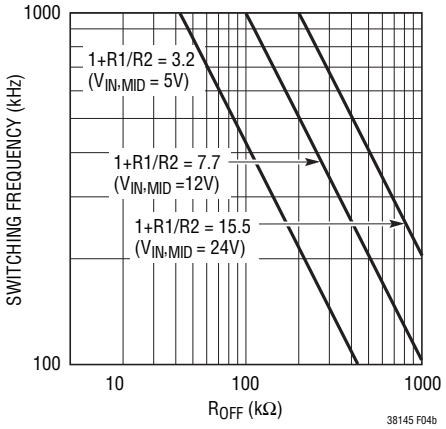


Figure 4b. Switching Frequency vs R_{OFF} (V_{OFF} Connected to a Resistor Divider from V_{IN})

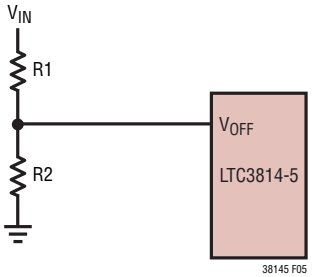


Figure 5. V_{OFF} Connection to Keep the Operating Frequency Constant as the Input Supply Varies

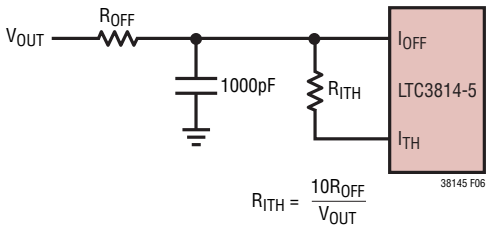


Figure 6. Correcting Frequency Shift with Load Current Changes

APPLICATIONS INFORMATION

Minimum On-Time and Dropout Operation

The minimum on-time $t_{ON(MIN)}$ is the smallest amount of time that the LTC3814-5 is capable of turning on the bottom MOSFET, tripping the current comparator and turning the MOSFET back off. This time is generally about 350ns. The minimum on-time limit imposes a minimum duty cycle of $t_{ON(MIN)}/(t_{ON(MIN)} + t_{OFF})$. If the minimum duty cycle is reached, due to a rising input voltage for example, then the output will rise out of regulation. The maximum input voltage to avoid dropout is:

$$V_{IN(MAX)} = V_{OUT} \frac{t_{OFF}}{t_{ON(MIN)} + t_{OFF}}$$

A plot of maximum duty cycle vs switching frequency is shown in Figure 7.

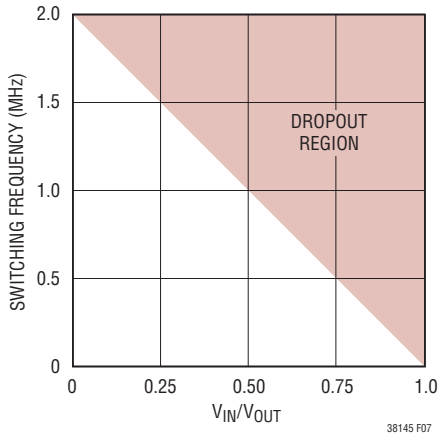


Figure 7. Maximum Switching Frequency vs Duty Cycle

Inductor Selection

An inductor should be chosen that can carry the maximum input DC current which occurs at the minimum input voltage. The peak-to-peak ripple current is set by the inductance and a good starting point is to choose a ripple current of at least 40% of its maximum value:

$$\Delta I_L = 40\% \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The required inductance can then be calculated to be:

$$L = \frac{V_{IN(MIN)} \bullet D_{MAX}}{f \bullet \Delta I_L}$$

The required saturation of the inductor should be chosen to be greater than the peak inductor current:

$$I_{L(SAT)} \geq \frac{I_{O(MAX)}}{1 - D_{MAX}} + \frac{\Delta I_L}{2}$$

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft and Toko.

Schottky Diode D1 Selection

The Schottky diode D1 shown in the front page schematic conducts during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diode of the synchronous MOSFET from turning on and storing charge during the dead time, which can cause a modest (about 1%) efficiency loss. The diode can be rated for about one half to one fifth of the full load current since it is on for only a fraction of the duty cycle. The peak reverse voltage that the diode must withstand is equal to the regulator output voltage. In order for the diode to be effective, the inductance between it and the synchronous MOSFET must be as small as possible, mandating that these components be placed adjacently. The diode can be omitted if the efficiency loss is tolerable.

Output Capacitor Selection

In a boost converter, the output capacitor requirements are demanding due to the fact that the current waveform is pulsed. The choice of component(s) is driven by the acceptable ripple voltage which is affected by the ESR, ESL and bulk capacitance as shown in Figure 8e. The total output ripple voltage is:

$$\Delta V_{OUT} = I_{O(MAX)} \left(\frac{1}{f \bullet C_{OUT}} + \frac{ESR}{1 - D_{MAX}} \right)$$

where the first term is due to the bulk capacitance and second term due to the ESR.

APPLICATIONS INFORMATION

For many designs it is possible to choose a single capacitor type that satisfies both the ESR and bulk C requirements for the design. In certain demanding applications, however, the ripple voltage can be improved significantly by connecting two or more types of capacitors in parallel. For example, using a low ESR ceramic capacitor can minimize the ESR step, while an electrolytic capacitor can be used to supply the required bulk C.

Once the output capacitor ESR and bulk capacitance have been determined, the overall ripple voltage waveform should be verified on a dedicated PC board (see PC Board Layout Checklist section for more information on component placement). Lab breadboards generally suffer from excessive series inductance (due to inter-component wiring), and these parasitics can make the switching waveforms look significantly worse than they would be on a properly designed PC board.

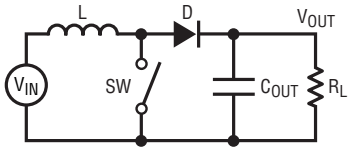
The output capacitor in a boost regulator experiences high RMS ripple currents, as shown in Figure 8d. The RMS output capacitor ripple current is:

$$I_{RMS(COUT)} \approx I_{O(MAX)} \bullet \sqrt{\frac{V_O - V_{IN(MIN)}}{V_{IN(MIN)}}}$$

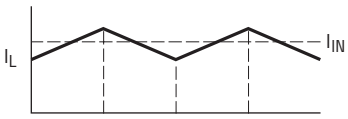
Note that the ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design.

Manufacturers such as Nichicon, Nippon Chemi-con and Sanyo should be considered for high performance throughhole capacitors. The OS-CON (organic semiconductor dielectric) capacitor available from Sanyo has the lowest product of ESR and size of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to reduce the effect of their lead inductance.

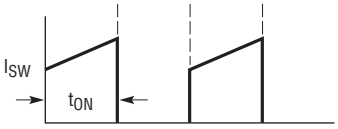
In surface mount applications, multiple capacitors placed in parallel may be required to meet the ESR, RMS current handling and load step requirements. Dry tantalum, special polymer and aluminum electrolytic capacitors are available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Several excellent surge-tested choices are the AVX TPS and TPSV or the KEMET T510 series. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-driven applications providing that consideration is given to ripple current ratings and long term reliability. Other capacitor types include Panasonic SP and Sanyo POSCAPs. In applications with V_{OUT} > 30V, however, choices are limited to aluminum electrolytic and ceramic capacitors.



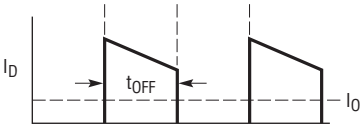
8a. Circuit Diagram



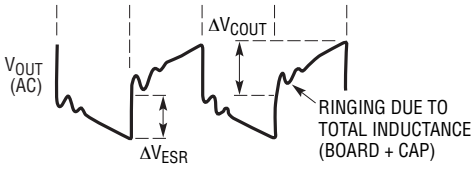
8b. Inductor and Input Currents



8c. Switch Current



8d. Diode and Output Currents



8e. Output Voltage Ripple Waveform 38145 F08

Figure 8. Switching Waveforms for a Boost Converter

APPLICATIONS INFORMATION

Input Capacitor Selection

The input capacitor of a boost converter is less critical than the output capacitor, due to the fact that the inductor is in series with the input and the input current waveform is continuous (see Figure 8b). The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 10µF to 100µF. A low ESR capacitor is recommended though not as critical as for the output capacitor.

The RMS input capacitor ripple current for a boost converter is:

$$I_{RMS(CIN)} = 0.3 \bullet \frac{V_{IN(MIN)}}{L \bullet f} \bullet D_{MAX}$$

Please note that the input capacitor can see a very high surge current when a battery is suddenly connected to the input of the converter and solid tantalum capacitors can fail catastrophically under these conditions. **Be sure to specify surge-tested capacitors!**

Output Voltage

The LTC3814-5 output voltage is set by a resistor divider according to the following formula:

$$V_{OUT} = 0.8V\left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

The external resistor divider is connected to the output as shown in the Functional Diagram, allowing remote voltage sensing. The resultant feedback signal is compared with the internal precision 800mV voltage reference by the error amplifier. The internal reference has a guaranteed tolerance of less than ±1%. Tolerance of the feedback resistors will add additional error to the output voltage. 0.1% to 1% resistors are recommended.

Top MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from $INTV_{CC}$ when the switch node is low. When the top MOSFET turns on, the switch node rises to V_{OUT} and the BOOST pin rises to approximately $V_{OUT} + INTV_{CC}$. The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

The reverse breakdown of the external diode, D_B, must be greater than V_{OUT}. Another important consideration for the external diode is the reverse recovery and reverse leakage, either of which may cause excessive reverse current to flow at full reverse voltage. If the reverse current times reverse voltage exceeds the maximum allowable power dissipation, the diode may be damaged. For best results, use an ultrafast recovery diode such as the MMDL770T1.

IC/MOSFET Driver Supplies ($INTV_{CC}$)

The LTC3814-5 drivers and the LTC3814-5 internal circuits are supplied from the $INTV_{CC}$ pin (see Figure 1). These pins have an operating range between 4.2V and 14V. If the input voltage or another supply is not available in this voltage range, two internal regulators are provided to simplify the generation of this IC/driver supply voltage as described in the next sections.

The N_{DRV} Pin Regulator

The N_{DRV} pin controls the gate of an external NMOS as shown in Figure 9b and can be used to generate a regulated 5.5V supply from V_{IN} or V_{OUT}. Since the NMOS is external, it can be chosen with a BV_{DSS} or power rating as high as necessary to safely derive power from a high voltage input or output voltage. In order to generate an $INTV_{CC}$ supply that is always above the 4.2V UV threshold, the supply connected to the drain must be greater than $4.2V + R_{NDRV} \bullet 40\mu A + V_T$.

The $EXTV_{CC}$ Pin Regulator

A second low dropout regulator is available for voltages ≤ 15V. When a supply that is greater than 4.7V is connected to the $EXTV_{CC}$ pin, the internal LDO will regulate 5.5V on $INTV_{CC}$ from the $EXTV_{CC}$ pin voltage and will also disable the NDRV pin regulator. This regulator is disabled when the IC is shut down, when $INTV_{CC} < 4.2V$, or when $EXTV_{CC} < 4.7V$.

APPLICATIONS INFORMATION

Using the $INTV_{CC}$ Regulators

One, both or neither of these regulators can be used to generate the 5.5V IC/driver supply depending on the circuit requirements, available supplies, and the voltage range of V_{IN} or V_{OUT}. Deriving the 5.5V supply from V_{IN} is more efficient, however deriving it from V_{OUT} has the advantage of maintaining regulation of V_{OUT} when V_{IN} drops below the UV threshold. Four possible configurations are shown in Figures 9a through 9d, and are described as follows:

1. Figure 9a. If the V_{IN} voltage or another low voltage supply between 4.5V and 14V is available, the simplest approach is to connect this supply directly to the $INTV_{CC}$ and DRV_{CC} pins. The internal regulators are disabled by shorting NDRV and $EXTV_{CC}$ to $INTV_{CC}$.
2. Figure 9b. If $V_{IN(MAX)}$ > 14V, an external NMOS connected to the NDRV pin can be used to generate 5.5V from V_{IN}. $V_{IN(MIN)}$ must be > 4.5V + R_{NDRV} • 40µA + V_T to keep $INTV_{CC}$ above the UV threshold and the BV_{DSS} of the external NMOS must be chosen to be greater than $V_{IN(MAX)}$. The $EXTV_{CC}$ regulator is disabled by grounding the $EXTV_{CC}$ pin.
3. Figure 9c. If the $V_{IN(MAX)}$ < 14.7V and V_{IN} is allowed to fall below 4.2V without disrupting the boost converter operation, use this configuration. The $INTV_{CC}$ supply is derived from V_{IN} until the V_{OUT} > 4.7V. Once $INTV_{CC}$ is derived from V_{OUT}, V_{IN} can fall below the 4V UV threshold without losing regulation of V_{OUT}. Note that in this configuration, V_{IN} must be > ~5V at least long enough to start up the LTC3814-5 and charge V_{OUT} > 4.7V. Also, since V_{OUT} is connected to the $EXTV_{CC}$ pin, this configuration is limited to V_{OUT} < 15V.
4. Figure 9d. Similar to configuration 3 except that V_{OUT} is allowed to be >15V since V_{OUT} is connected to an external NMOS with appropriately rated BV_{DSS}. V_{IN} has same start-up requirement as 3.

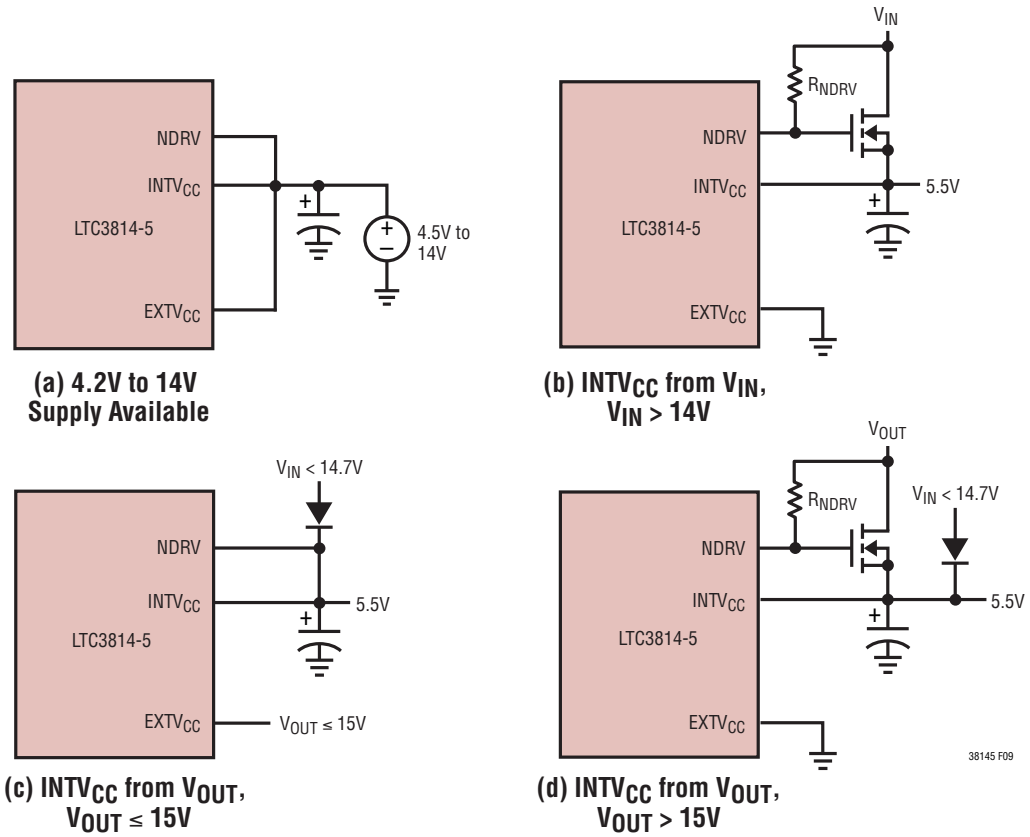


Figure 9. Four Possible Ways to Generate $INTV_{CC}$ Supply

APPLICATIONS INFORMATION

Power Dissipation Considerations

Applications using large MOSFETs and high frequency of operation may result in a large $DRV_{CC}/INTV_{CC}$ supply current. Therefore, when using the linear regulators, it is necessary to verify that the resulting power dissipation is within the maximum limits. The $DRV_{CC}/INTV_{CC}$ supply current consists of the MOSFET gate current plus the LTC3814-5 quiescent current:

$$I_{CC} = (f)(Q_{G(TOP)} + Q_{G(BOTTOM)}) + 3mA$$

When using the internal LDO regulator, the power dissipation is internal so the rise in junction temperature can be estimated from the equation given in Note 2 of the Electrical Characteristics as follows:

$$T_J = T_A + I_{EXTVCC} \bullet (V_{EXTVCC} - V_{INTVCC})(38°C/W)$$

and must not exceed 125°C.

Likewise, if the external NMOS regulator is used, the worst case power dissipation is calculated to be:

$$P_{MOSFET} = (V_{DRAIN(MAX)} - 5.5V) \bullet I_{CC}$$

and can be used to properly size the device.

FEEDBACK LOOP/COMPENSATION

Introduction

In a typical LTC3814-5 circuit, the feedback loop consists of two sections: the modulator/output stage and the feedback amplifier/compensation network. The modulator/output stage consists of the current sense component and internal current comparator, the power MOSFET switches and drivers, and the output filter and load. The transfer function of the modulator/output stage for a boost converter consists of an output capacitor pole, R_LC_{OUT}, and an ESR zero, $R_{ESR}C_{OUT}$, and also a "right-half plane" zero, $(R_L/L)(V_{IN}^2/V_{OUT}^2)$. It has a gain/phase curve that is typically like the curve shown in Figure 10 and is expressed mathematically in the following equation.

$$H(s) = \frac{V_{OUT}(s)}{V_{ITH}(s)} = \left(\frac{R_L \bullet V_{IN} \bullet V_{SENSE(MAX)}}{2.4 \bullet V_{OUT} \bullet R_{DS(ON)}}\right) \bullet \left(\frac{1 + s \bullet R_{ESR} \bullet C_{OUT}}{1 + s \bullet R_L \bullet C_{OUT}}\right) \bullet \left(1 - s \bullet \frac{L}{R_L} \bullet \frac{V_{OUT}^2}{V_{IN}^2}\right) \quad (1)$$

$$s = j2\pi f$$

This portion of the power supply is pretty well out of the user's control since the current sense is chosen based on maximum output load, and the output capacitor is usually chosen based on load regulation and ripple requirements without considering AC loop response. The feedback amplifier, on the other hand, gives us a handle on which to adjust the AC response. The goal is to have an 180° phase shift at DC so the loop regulates and less than 360° phase shift at the point where the loop gain falls below 0dB, i.e., the crossover frequency, with as much gain as possible at frequencies below the crossover frequency. Since the feedback amplifier adds an additional 90° phase shift to the phase shift already present from the modulator/output stage, some phase boost is required at the crossover frequency to achieve good phase margin. The design procedure (described in more detail in the next section) is to (1) obtain a gain/phase plot of modulator/output stage, (2) choose a crossover frequency and the required phase boost, and (3) calculate the compensation network.

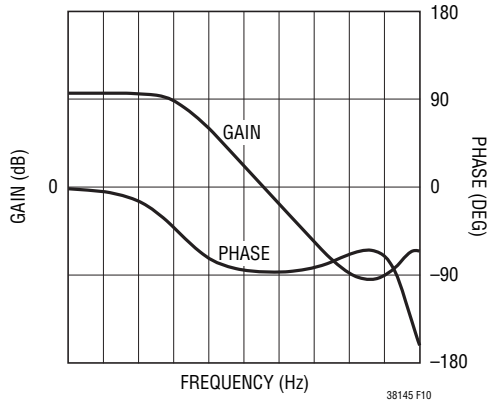


Figure 10. Bode Plot of Boost Modulator/Output Stage

APPLICATIONS INFORMATION

The two types of compensation networks, Type 2 and Type 3 are shown in Figures 11 and 12. When component values are chosen properly, these networks provide a "phase bump" at the crossover frequency. Type 2 uses a single pole-zero pair to provide up to about 60° of phase boost while Type 3 uses two poles and two zeros to provide up to 150° of phase boost.

The compensation of boost converters are complicated by two factors: the RHP zero and the dependence of the loop gain on the duty cycle. The RHP zero adds additional phase lag and gain. The phase lag degrades phase margin and the added gain keeps the gain high typically in the frequency region where the user is trying the roll off the gain below 0dB. This often forces the user to choose a crossover frequency at a lower frequency than originally desired. The duty cycle effect of gain (see above transfer function) causes the phase margin and crossover frequency to be dependent on the input supply voltage which may cause problems if the input voltage varies over a wide range since the compensation network can only be optimized for a specific crossover frequency. These two factors usually can be overcome if the crossover frequency is chosen low enough.

Feedback Component Selection

Selecting the R and C values for a typical Type 2 or Type 3 loop is a nontrivial task. The applications shown in this data sheet show typical values, optimized for the power components shown. They should give acceptable performance with similar power components, but can be way off if even one major power component is changed significantly. Applications that require optimized transient response will require recalculation of the compensation values specifically for the circuit in question. The underlying mathematics are complex, but the component values can be calculated in a straightforward manner if we know the gain and phase of the modulator at the crossover frequency.

Modulator gain and phase can be obtained in one of three ways: measured directly from a breadboard, or if the appropriate parasitic values are known, simulated or generated from the modulator transfer function. Measurement will give more accurate results, but simulation or transfer function can often get close enough to give a working system. To measure the modulator gain and phase directly, wire up a breadboard with an LTC3814-5 and the actual MOSFETs, inductor and input and output capacitors that the final design will use. This breadboard should use appropriate construction techniques for high speed analog circuitry: bypass capacitors located close to the LTC3814-5, no long wires connecting components, appropriately sized ground returns, etc. Wire the feedback amplifier with a 0.1µF feedback capacitor from I_{TH} to FB and a 10k to 100k resistor from V_{OUT} to FB. Choose the bias resistor (R_B) as required to set the desired output voltage. Disconnect R_B from ground and connect it to a signal generator or to the source output of a network analyzer to inject a test signal into the loop. Measure the gain and phase from the I_{TH} pin to the output node at the positive terminal of the output capacitor. Make sure the analyzer's input is AC coupled so that the DC voltages present at both the I_{TH} and V_{OUT} nodes don't corrupt the measurements or damage the analyzer.

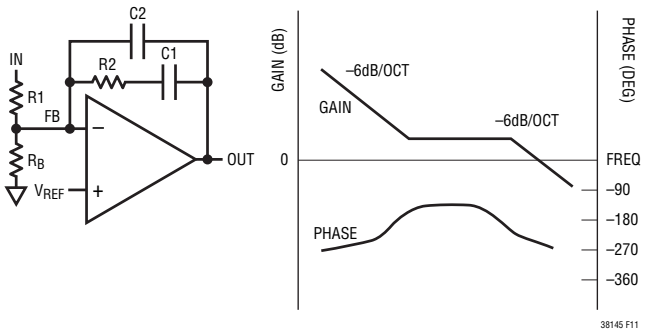


Figure 11. Type 2 Schematic and Transfer Function

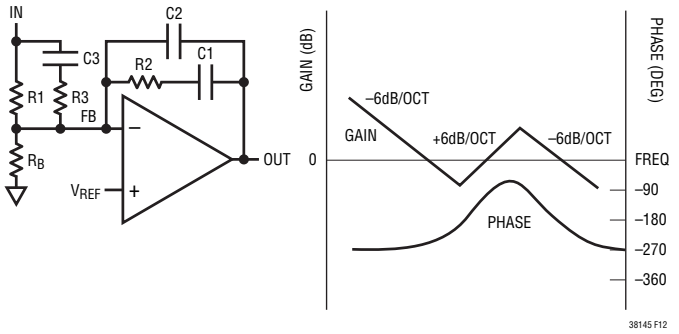


Figure 12. Type 3 Schematic and Transfer Function

APPLICATIONS INFORMATION

If breadboard measurement is not practical, mathematical software such as MATHCAD or MATLAB can be used to generate plots from the transfer function given in Equation 1. A SPICE simulation can also be used to generate approximate gain/phase curves. Plug the expected capacitor, inductor and MOSFET values into the following SPICE deck and generate an AC plot of V_{OUT}/V_{ITH} with gain in dB and phase in degrees. Refer to your SPICE manual for details of how to generate this plot.

```
*This file simulates a simplified model of
the 3814-5 for generating a v(out)/(vith) or
a v(out)/v(outin) bode plot

.param vout=24
.param vin=12
.param L=10u
.param cout=270u
.param esr=.018
.param rload=24
*
.param rdson=0.02
.param Vrng=1
.param vsnsmax={0.173*Vrng-0.026}
.param K={vsnsmax/rdson/1.2}
.param wz={1/esr/cout}
.param wp={2/rload/cout}
*
* Feedback Amplifier
rfb1 outin vfb 29k
rfb2 vfb 0 1k
eithx ithx 0 laplace {0.8-v(vfb)} =
  {1/(1+s/1000)}
eith ith 0 value={limit(1e6*v(ithx),0,2.4)}
cc1 ith vfb 100p
cc2 ith x1 0.01p
rc x1 vfb 100k
*
* Modulator/Output Stage
eout out 0 laplace {v(ith)} =
  {0.5*K*Rload*vin/vout *(1+s/wz)/(1+s/wp)
  *(1-s*L/Rload*vout*vout/vin/vin)}
rload out 0 {rload}
*
vstim out outin dc=0 ac=10m; ac stimulus
.ac dec 100 10 10meg
.probe
.end
```

With the gain/phase plot in hand, a loop crossover frequency can be chosen. Usually the curves look something like Figure 10. Choose the crossover frequency about 25% of the switching frequency for maximum bandwidth. Although it may be tempting to go beyond $f_{SW}/4$, remember that significant phase shift occurs at half the switching frequency that isn't modeled in the above H(s) equation and PSPICE code. Note the gain (GAIN, in dB) and phase (PHASE, in degrees) at this point. The desired feedback amplifier gain will be –GAIN to make the loop gain at 0dB at this frequency. Now calculate the needed phase boost, assuming 60° as a target phase margin:

BOOST = – (PHASE + 30°)

If the required BOOST is less than 60°, a Type 2 loop can be used successfully, saving two external components. BOOST values greater than 60° usually require Type 3 loops for satisfactory performance.

Finally, choose a convenient resistor value for R1 (10k is usually a good value). Now calculate the remaining values:

(K is a constant used in the calculations)

f = chosen crossover frequency

$G = 10^{(GAIN/20)}$ (this converts GAIN in dB to G in absolute gain)

APPLICATIONS INFORMATION

TYPE 2 Loop:

$$K = \tan\left(\frac{BOOST}{2} + 45^\circ\right)$$

$$C2 = \frac{1}{2\pi \bullet f \bullet G \bullet K \bullet R1}$$

$$C1 = C2\left(K^2 - 1\right)$$

$$R2 = \frac{K}{2\pi \bullet f \bullet C1}$$

$$R_B = \frac{V_{REF}(R1)}{V_{OUT} - V_{REF}}$$

TYPE 3 Loop:

$$K = \tan^2\left(\frac{BOOST}{4} + 45^\circ\right)$$

$$C2 = \frac{1}{2\pi \bullet f \bullet G \bullet R1}$$

$$C1 = C2\left(K - 1\right)$$

$$R2 = \frac{\sqrt{K}}{2\pi \bullet f \bullet C1}$$

$$R3 = \frac{R1}{K - 1}$$

$$C3 = \frac{1}{2\pi f \sqrt{K} \bullet R3}$$

$$R_B = \frac{V_{REF}(R1)}{V_{OUT} - V_{REF}}$$

SPICE or mathematical software can be used to generate the gain/phase plots for the compensated power supply to do a sanity check on the component values before trying them out on the actual hardware. For software, use the following transfer function:

T(s) = A(s)H(s)

where H(s) was given in equation 2 and A(s) depends on compensation circuit used:

Type 2:

$$A(s) = \frac{1 + s \bullet R2 \bullet C1}{s \bullet R1 \bullet (C1 + C2) \bullet \left(1 + s \bullet R2 \bullet \frac{C1 \bullet C2}{C1 + C2}\right)}$$

Type 3:

$$A(s) = \frac{1}{s \bullet R1 \bullet (C1 + C2)} \bullet \frac{(1 + s \bullet (R1 + R3) \bullet C3) \bullet (1 + s \bullet R2 \bullet C1)}{(1 + s \bullet R3 \bullet C3) \bullet \left(1 + s \bullet R2 \bullet \frac{C1 \bullet C2}{C1 + C2}\right)}$$

For SPICE, simulate the previous PSPICE code with calculated compensation values entered and generate a gain/phase plot of V_{OUT}/V_{OUTIN}.

Fault Conditions: Current Limit

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3814-5, the maximum sense voltage is controlled by the voltage on the V_{RNG} pin. With peak current control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{LIMIT} = \frac{V_{SNS(MAX)}}{R_{DS(ON)}\ \rho_T} - \frac{1}{2}\Delta I_L$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The minimum value of current limit generally occurs at the lowest V_{IN} at the highest ambient temperature, conditions that cause the largest power loss in the converter. Note that it is important to check for self-consistency between the assumed MOSFET junction temperature and the resulting value of I_{LIMIT} which heats the MOSFET switches.

Caution should be used when setting the current limit based upon the $R_{DS(ON)}$ of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for $R_{DS(ON)}$, but not a minimum.

APPLICATIONS INFORMATION

A reasonable assumption is that the minimum $R_{DS(ON)}$ lies the same percentage below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

Note that in a boost mode architecture, it is only possible to provide protection for "soft" shorts where $V_{OUT} > V_{IN}$. For hard shorts, the inductor current is limited only by the input supply capability.

Run/Soft-Start Function

The RUN/SS pin is a multipurpose pin that provides a soft-start function and a means to shut down the LTC3814-5. Soft-start reduces the input supply's surge current by controlling the ramp rate of the I_{TH} voltage, eliminates output overshoot and can also be used for power supply sequencing.

Pulling RUN/SS below 0.9V puts the LTC3814-5 into a low quiescent current shutdown (I_Q = 224µA). This pin can be driven directly from logic as shown in Figure 14. Releasing the RUN/SS pin allows an internal 1.4µA current source to charge up the soft-start capacitor, C_{SS}. When the voltage on RUN/SS reaches 0.9V, the LTC3814-5 turns on and begins ramping the I_{TH} voltage at $V_{ITH} = V_{SS} – 0.9V$. As the RUN/SS voltage increases from 0.9V to 3.3V, the current limit is increased from 0% to 100% of its maximum value. The RUN/SS voltage continues to charge until it reaches its internally clamped value of 4V.

If RUN/SS starts at 0V, the delay before starting is approximately:

$$t_{DELAY,START} = \frac{0.9V}{1.4\mu A} C_{SS} = (0.64s/\mu F) C_{SS}$$

plus an additional delay, before the current limit reaches its maximum value of:

$$t_{DELAY,REG} \geq \frac{2.4V}{1.4\mu A} C_{SS}$$

The start delay can be reduced by using diode D1 in Figure 13.

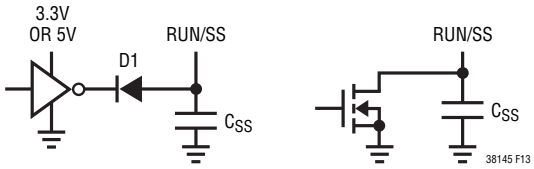


Figure 13. RUN/SS Pin Interfacing

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3814-5 circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high input currents. The input current is maximum at maximum output current and minimum input voltage. The average input current flows through L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and the board traces to obtain the DC I^2R loss. For example, if $R_{DS(ON)}$ = 0.01Ω and R_L = 0.005Ω, the loss will range from 15mW to 1.5W as the input current varies from 1A to 10A.
2. Transition loss. This loss arises from the brief amount of time the bottom MOSFET spends in the saturated region during switch node transitions. It depends upon the output voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at output voltages above 20V and can be estimated from the second term of the P_{MAIN} equation found in the Power MOSFET Selection section. When transition losses are significant, efficiency can be improved by lowering the frequency and/or using a bottom MOSFET(s) with lower C_{RSS} at the expense of higher $R_{DS(ON)}$.
3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents. Control current is typically

APPLICATIONS INFORMATION

about 3mA and driver current can be calculated by: $I_{GATE} = f(Q_{G(TOP)} + Q_{G(BOT)})$, where $Q_{G(TOP)}$ and $Q_{G(BOT)}$ are the gate charges of the top and bottom MOSFETs. This loss is proportional to the supply voltage that $INTV_{CC}$ is derived from, i.e., V_{IN}, V_{OUT} or an external supply connected to $INTV_{CC}$.

4. C_{OUT} loss. The output capacitor has the difficult job of filtering the large RMS input current out of the synchronous MOSFET. It must have a very low ESR to minimize the AC I^2R loss.

Other losses, including C_{IN} ESR loss, Schottky diode D1 conduction loss during dead time and inductor core loss generally account for less than 2% additional loss. When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Design Example

As a design example, take a supply with the following specifications: V_{IN} = 12V ±20%, V_{OUT} = 24V ±5%, $I_{OUT(MAX)}$ = 5A, f = 250kHz. Since V_{IN} can vary around the 12V nominal value, connect a resistive divider from V_{IN} to V_{OFF} to keep the frequency independent of V_{IN} changes:

$$\frac{R1}{R2} = \frac{12V}{1.55V} - 1 = 6.74$$

Choose R1 = 133k and R2 = 20k. Now calculate timing resistor R_{OFF}:

$$R_{OFF} = \frac{1 + 133k / 20k}{250kHz \bullet 76pF} = 402.6k$$

The duty cycle is:

$$D = 1 - \frac{12V}{24V} = 0.5$$

and the maximum input current is:

$$I_{IN(MAX)} = \frac{5A}{1 - 0.5} = 10A$$

Choose the inductor for about 40% ripple current at the maximum V_{IN}:

$$L = \frac{12V}{250kHz \bullet 0.4 \bullet 10A}\left(1 - \frac{12V}{24V}\right) = 6\mu H$$

The peak inductor current is:

$$I_{L(PEAK)} = \frac{5A}{1 - 0.5} + \frac{1}{2}(4A) = 12A$$

so, choose the CDEP147 5.9µH inductor with I_{SAT} = 16.4A at 100°C.

Next, choose the bottom MOSFET switch. Since the drain of the MOSFET will see the full output voltage plus any ringing, choose a 40V MOSFET to provide a margin of safety. The Si7848DP has:

BV_{DSS} = 40V
$R_{DS(ON)}$ = 9mΩ(max)/7.5mΩ(nom),
δ = 0.006/°C,
C_{MILLER} = (14nC – 6nC)/20V = 400pF,
$V_{GS(MILLER)}$ = 3.5V,
θ_{JA} = 20°C/W.

This yields a nominal sense voltage of:

$$V_{SNS(NOM)} = \frac{1.7 \bullet 0.0075\Omega \bullet 5A}{1 - 0.5} = 128mV$$

APPLICATIONS INFORMATION

To guarantee proper current limit at worst-case conditions, increase nominal V_{SNS} by 50% to 190mV. To check if the current limit is acceptable at V_{SNS} = 190mV, assume a junction temperature of about 30°C above a 70°C ambient ($\rho_{100°C}$ = 1.4):

$$I_{IN(MAX)} \geq \frac{190mV}{1.4 \bullet 0.009\Omega} - \frac{1}{2} \bullet 4A = 13A$$

$I_{OUT(MAX)} = I_{IN(MAX)} \bullet (1\text{-}D_{MAX}) = 6.5A$

and double-check the assumed T_J in the MOSFET:

$$P_{TOP} = \left(\frac{1}{1-0.5}\right)(6.5A)^2(1.4)(0.009\Omega) = 1.06W$$

T_J = 70°C + 1.06W • 20°C/W = 91°C

Verify that the Si7848DP is also a good choice for the bottom MOSFET by checking its power dissipation at current limit and minimum input voltage, assuming a junction temperature of 30°C above a 70°C ambient ($\rho_{100°C}$ = 1.4):

$$P_{BOT} = 0.5\left(\frac{6.5A}{1-0.5}\right)^2(1.4)(0.009\Omega)$$
$$+ \frac{1}{2}(24V)^2\left(\frac{6.5A}{1-0.5}\right)(2)(400pF)$$
$$\bullet\left(\frac{1}{12V-3.5V} + \frac{1}{3.5V}\right)(250kHz)$$
$$= 1.06W + 0.30W = 1.36W$$

T_J = 70°C + 1.36W • 20°C/W = 97°C

The junction temperature will be significantly less at nominal current, but this analysis shows that careful attention to heat sinking on the board will be necessary in this circuit.

Since V_{IN} is always between 4.5V and 14V, it can be connected directly to the $INTV_{CC}$ and DRV_{CC} pins.

C_{OUT} is chosen for an RMS current rating of about 5A at 85°C. The output capacitors are chosen for a low ESR of 0.018Ω to minimize output voltage changes due to inductor ripple current and load steps. The ripple voltage will be only:

$$\Delta V_{OUT(RIPPLE)} = (5A)\left(\frac{1}{250kHz \bullet 330\mu F} + \frac{0.018}{1-0.5}\right)$$
$$= 0.25V \text{ (about 1\%)}$$

A 0A to 5A load step will cause an output change of up to:

$\Delta V_{OUT(STEP)} = \Delta I_{LOAD} \bullet ESR = 5A \bullet 0.018\Omega$
$= 90mV$

An optional 10µF ceramic output capacitor is included to minimize the effect of ESL in the output ripple. The complete circuit is shown in Figure 14.

APPLICATIONS INFORMATION

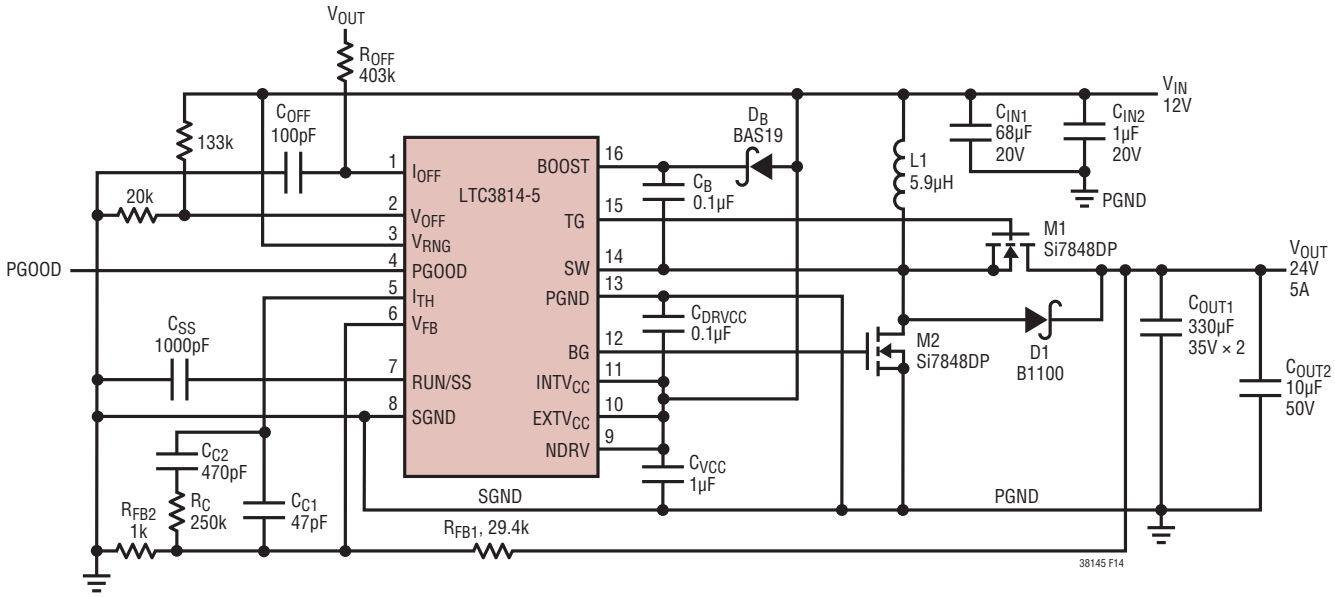


Figure 14. 12V Input Voltage to 24V/5A

APPLICATIONS INFORMATION

PC Board Layout Checklist

When laying out a PC board follow one of two suggested approaches. The simple PC board layout requires a dedicated ground plane layer. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

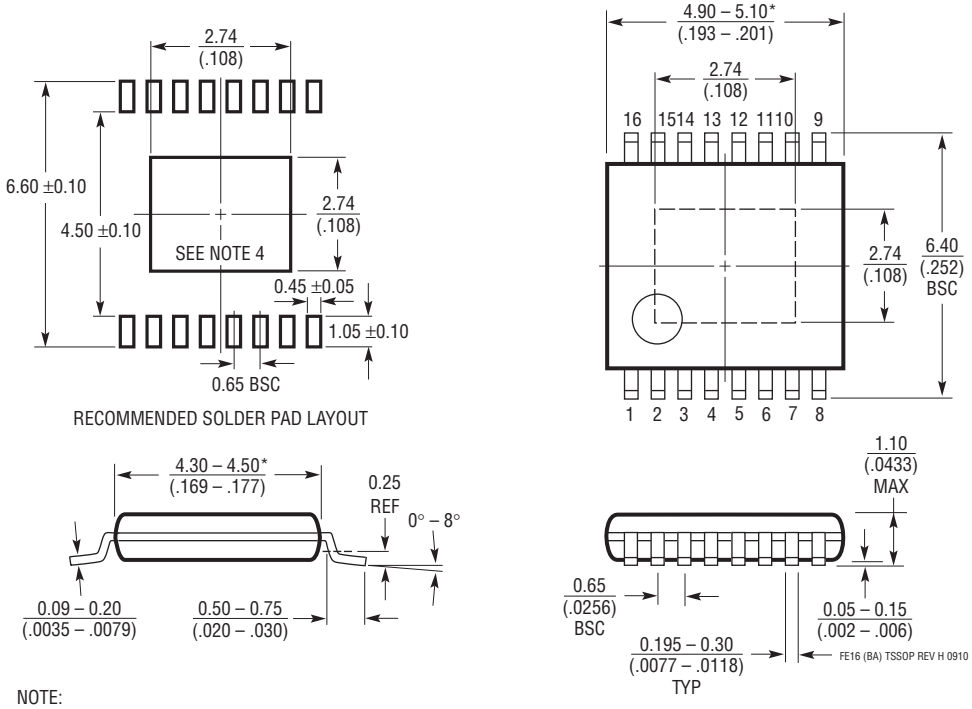
- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, C_{OUT}, MOSFETs, D1 and inductor all in one compact area. It may help to have some components on the bottom side of the board.
- Use an immediate via to connect the components to ground plane including SGND and PGND of LTC3814-5. Use several bigger vias for power components.
- Use compact plane for switch node (SW) to improve cooling of the MOSFETs and to keep EMI down.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component. You can connect the copper areas to any DC net (V_{IN}, V_{OUT}, GND or to any other DC rail in your system).

When laying out a printed circuit board, without a ground plane, use the following checklist to ensure proper operation of the controller.

- Segregate the signal and power grounds. All small signal components should return to the SGND pin at one point which is then tied to the PGND pin close to the source of M2.
- Place M2 as close to the controller as possible, keeping the PGND, BG and SW traces short.
- Connect the input capacitor(s) C_{IN} close to the power MOSFETs. This capacitor carries the MOSFET AC current.
- Keep the high dV/dt SW, BOOST and TG nodes away from sensitive small-signal nodes.
- Connect the $INTV_{CC}$ decoupling capacitor C_{VCC} closely to the $INTV_{CC}$ and SGND pins.
- Connect the top driver boost capacitor C_B closely to the BOOST and SW pins.
- Connect the bottom driver decoupling capacitor C_{INTVCC} closely to the $INTV_{CC}$ and PGND pins.

PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev H)
Exposed Pad Variation BA



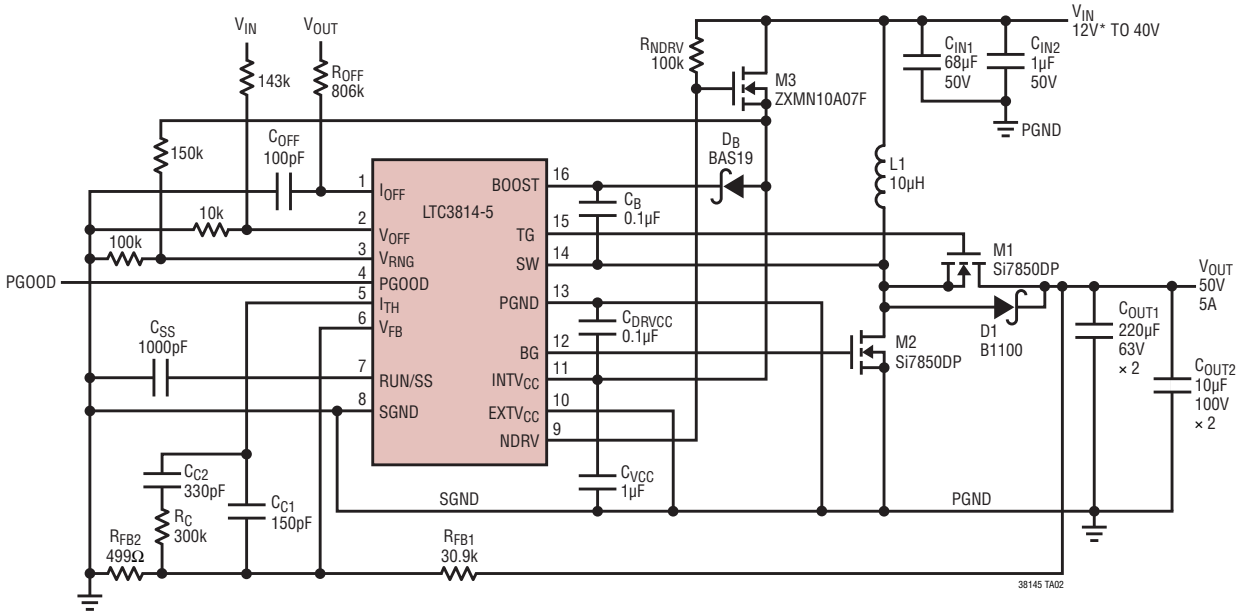
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	01/11	Updated Description section	1
		Changed Operating Junction Temperature Range in Absolute Maximum Ratings and Order Information sections	2
		Remove Lead Based Part Numbers from Order Information	2
		Updated Note 2	4
		Updated Fault Monitoring/Protection section	10
		Updated Equations	22
		Updated Related Parts	30

TYPICAL APPLICATION

24V Input Voltage to 50V/5A



*$I_{OUT(MAX)}$ = 2A AT V_{IN} = 12V

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3786	Low I_Q Synchronous Boost Controller	2.5V ≤ V_{IN} ≤ 38V, V_{OUT} up to 60V, Fixed Operating Frequency 50kHz to 900kHz, MSOP-16E, 3mm × 3mm QFN-16
LTC3787	2-Phase, Single Output Synchronous Step-Up Controller	2.5V ≤ V_{IN} ≤ 38V, V_{OUT} up to 60V, 50kHz to 900kHz, SSOP-28, 4mm × 5mm QFN-28
LTC3788/LTC3788-1	2-Phase, Dual Output Synchronous Step-Up Controller	2.5V ≤ V_{IN} ≤ 38V, V_{OUT} up to 60V, 50kHz to 900kHz, SSOP-28
LTC3862/LTC3862-1	2-Phase Current Mode Step-Up DC/DC Controller	4V ≤ V_{IN} ≤ 36V, 5V or 10V Gate Drive, 75kHz to 500kHz
LTC3813	100V Maximum V_{OUT} Synchronous Step-Up DC/DC Controller	No R_{SENSE}, Large 1Ω Gate Driver, Adjustable Off-Time, SSOP-28
LTC1871, LTC1871-1, LTC1871-7	Wide Input Range, No R_{SENSE} Low Quiescent Current Flyback, Boost and SEPIC Controller	Adjustable Switching Frequency, 2.5V ≤ V_{IN} ≤ 36V, Burst Mode Operation at Light Load, MSOP-10
LT3757	Boost, Flyback, SEPIC and Inverting Controller	2.9V ≤ V_{IN} ≤ 40V, 100kHz to 1MHz Programmable Operation Frequency, 3mm × 3mm DFN-10 and MSOP-10E
LT3758	Boost, Flyback, SEPIC and Inverting Controller	5.5V ≤ V_{IN} ≤ 100V, 100kHz to 1MHz Programmable Operation Frequency, 3mm × 3mm DFN-10 and MSOP-10E

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LT 0111 REV C • PRINTED IN USA

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